COURSE STRUCTURE FOR M.E. (E & TC/ELECTRONICS)- (VLSI and Embedded Systems)
(For 2008 course) (w.e.f. June – 2008)

SEMESTER I

CODE	SUBJECT	TEACHING SCHEME		EXAMINATION SCHEME					CREDITS
		Lect.	Pr.	Paper	TW	Oral	Pr	Total	
504181	Analog and Digital CMOS IC Design	3	-	100	-	-	-	100	3
504182	Principles and Practices for IT Management	3	-	100	-	-	-	100	3
504183	Embedded System Design	3	-	100	-	-	-	100	3
504184	Elective I	3	-	100	-	-	-	100	3
504185	Elective II	3	-	100	-	-	-	100	3
504186	VLSI Embedded Practice I	-	6	-	50	-	-	50	3
504187	Seminar I	-	4	-	50	-	-	50	2
Total of First Term		15	10	500	100	-	-	600	20

SEMESTER II

CODE	SUBJECT	TEACHING SCHEME		EXAMINATION SCHEME					CREDITS
		Lect.	Pr.	Paper	TW	Oral	Pr	Total	
504188	Real Time Operating Systems	3	-	100	-	-	-	100	3
504189	Embedded Signal Processing	3	-	100	-	-	-	100	3
504190	RF IC Design	3	-	100	-	-	-	100	3
504191	Elective III	3	-	100	-	-	-	100	3
504192	Elective IV (Open)	3	-	100	-	-	-	100	3
504193	VLSI Embedded Practice II	-	6	-	50	-	-	50	3
504194	Seminar II	-	4	-	50	-	-	50	2
Total of Second Term		15	10	500	100	-	-	600	20

SEMESTER III

CODE	SUBJECT	TEACHING SCHEME		EXAMINATION SCHEME					CREDITS
		Lect.	Pr.	Paper	TW	Oral	Pr	Total	
604181	Seminar III	-	4	-	50	-	-	50	2
604182	Project Stage I	-	18	-	50	-	-	50	6
Total of Third Term		-	22	-	100	-	-	100	8

SEMESTER IV

CODE	**SUBJECT**	**TEACHING SCHEME**		**EXAMINATION SCHEME**					**CREDITS**
		Lect.	**Pr.**	**Project**	**TW**	**Oral**	**Pr**	**Total**	
604183	Project Stage II	-	18	150*	-	50	-	200	12
Total of Fourth Term		-	18	150	-	50	-	200	12

* The Term Work of Project stage II of semester IV should be assessed jointly by the pair of internal and external examiners. along with the oral examination of the same.

Note : The Contact Hours for the calculation of load of teacher Seminar – 1Hr / week / student & Project – 2Hr / week / student

Elective I:

1. ASIC Design and Modeling
2. Nanotechnology
3. Machine Intelligence

Elective II:

1. Reconfigurable Computing
2. Memory Technologies
3. VLSI EDA Tools

Elective III:

1. Fault Tolerant System Design
2. Biomedical Signals and Systems
3. Advanced Digital System Design

Elective IV (OPEN):

1. Embedded Automotive Systems
2. System-on-Chip (SoC)
3. Software Defined Radio

Or any one subject of Elective IV from the following branches

1. Computer Engineering
2. Information Technology

504181 ANALOG AND DIGITAL CMOS IC DESIGN

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

MOS Switch, MOS Diode/ Active Resistor, Current Sinks & Sources, Current Mirror, Current & Voltage Reference, Band gap References. Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifier Architectures. Buffered Opamp, High Speed/Frequency Opamps, Differential Output Opamps, Micro power Op amps, Low Noise Opamp. Low Voltage Opamp, Macro models for Opamps. Sequential Ckts. Design of FSM, Moore & Mealy machines, Metastability, Solutions to metastability, Synchronization methods, VHDL codes for complex sequential machines, Hazards, Types of hazards, Method to eliminate hazards, case studies. CMOS parasitic, Technology scaling, Lambda parameter, Design calculations for different logic ckts, Calculations for Area on chip, Power dissipation, PDP, Transmission gate, Domino logic, NORA logic, CMOS layout techniques, Transient response, Advance trends of elements & Alloys for ultra fast logic ckts.

References:

1. Yusuf Leblebici, “CMOS Digital IC”,
2. Douglas Holberg, “CMOS Analog circuit design”, Oxford Publication.
3. Rabey, Chandrakasan, “Digital IC Design”.
4. Charls Roth, “Digital system Design using VHDL”, TMH.

504182 PRINCIPLES AND PRACTICES FOR IT MANAGEMENT

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

1. Management Perspectives

Role and importance of management, process of management – planning, organizing, staffing, directing, controlling. Nature, purpose and principles of management, Business policy, tools and techniques of strategic management, business ethics and social responsibilities

2. Preliminary planning of an IT Project

Gathering project Information, defining the project goals, establishing project priorities, requirements analysis, risk management, budgeting a project, creating a work breakdown structure, estimation

3. Organizing an IT Project

Organizing a Project Team: - Assessing internal scales, creating a team, managing team issues, resources procurement

Preparing and Implementing the project plan: - Defining the project schedule, project network diagram creation and analysis, project constraints, tracking project progress and financial obligations

Revising the project plan:-need for revision, establishing change control, implementing the project changes, coping with project delays

4. Group Dynamics and Team Management

Theories of Group Formation –Formal and Informal Groups and their interaction, Importance of teams - Formation of teams – Team Work, Leading the team, Team Meeting. Conflict Management - Traditional vis-à-vis Modern view of conflict, Conflict Process - Strategies for resolving destructive conflict, Stress management, employee welfare, energy management and energy audit,

5. Modern approaches to management

Concept of Knowledge management**,** change management, technology management, supply chain management, introduction to Intellectual property Rights (IPR)and cyber laws, process and project quality standards – six sigma, CMM, CMMI, PCMM, Impact of IT quality management systems, learning organizations

6. Applications of IT in management

Application of IT in functions like finance and accounting, stores, purchase, product design and development, quality control, logistics, customer relationship, marketing, project management, health care, insurance, banking, agriculture and service sector.

Reference Books:

1. Joseph Phillips, “IT Project Management”, Tata McGraw-Hill 2003 Edition
2. Management-Tasks, Responsibilities and practices, Peter Drucker
3. Management Theory and Practice- Ernst Dale
4. Management Information System-Javadekar
5. Business Policy- Azhar Kazmi
6. Industrial Energy Conservation- D.A.Ray, Pergamon Press
7. Resisting Intellectual Property-Halbert, Taylor & Francis Ltd ,2007

504183 EMBEDDED SYSTEM DESIGN

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Digital Systems and Embedded Systems, Design Methodology, Design Metrics, Specialties, Concepts & types of Memory, Cache Memory, Cache mapping techniques, replacement policies, Cache wire Techniques, Cache Impact on system Performance, Integrated Circuits Technologies-Full custom/VLSI, Logic Families, ASICs , PLDs, PALs, CPLDs , FPGA, Packaging and Circuit Boards, Interconnection and Signal Integrity , Differential Signaling. General Purpose Processor, System On chip, Embedded Computer Organization, ARM 7/ARM 9 architecture, ARM Microcontrollers and Processor Cores, Instructions and Data handling, interfacing with Memory, Interrupts, Timers, ARM Bus. I/O Devices, Controllers, Simple & Autonomous I/O Controllers, Parallel, Multiplexed, Tristate, and Open-Drain Buses, Bus Protocols, Serial Transmission Techniques & Standards, Wireless protocols, CAN & advanced Buses. Design Methodology, Design Flow, Architecture Exploration, Functional Design, Functional Verification, Synthesis, Physical Design, Design Optimization, Area Optimization, Timing Optimization, Power Optimization, Design for Test , Fault Models and Fault Simulation, Scan Design and Boundary Scan, Built-In Self Test (BIST), Nontechnical Issues.

References:

1. Digital Design: An Embedded Systems Approach Using Verilog, Peter J. Ashenden ELSEVIER, Morgan Kaufmann Publication, 2008.
2. Embedded Real Time Systems: Concepts, Design & Programming, Dr. K.V.K.K. Prasad, Dreamtech Publication
3. Embedded System Design: A unified Hardware/Software Introduction, Frank Vahid, and Tony Givargis.
4. Data books of ARM7/ARM9 J. Staunstrup and W. Wolf, editors, Hardware/Software Co-Design: Principles and Practice, Kluwer Academic Publishers, 1997.
5. G. DeMicheli, R. Ernst, and W. Wolf, editors, Readings in Hardware/Software Co-Design, Academic Press, 2002.

504184 ELECTIVE I
ASIC DESIGN AND MODELING

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Introduction to ASIC, Modeling combinational and sequential circuits, Design entry by verilog / VHDL /FSM / SYSTEM C, Hardware modeling with Verilog / VHDL, different verilog /VHDL constructs, and Logic Synthesis. ASIC construction, Simulation ,Verification of complex logic design model, Verification issues like verification plan, verification methodology, timing verification, Hardware design verification, Software design verification ,verification strategy for ASIC bus functional models, verification Automation, physical verification, Layout planning and verifications ,ASIC design flow and HDL based ASIC design flow, EDA tools for ASIC design, Mixed signal design , Introduction to VLSI physical design, floor planning , placement and routing parameter extraction , static timing analysis , current analysis , clock tree synthesis , power grid analysis , clock skew analysis and post layout synthesis , Data structure for graph models, , different tools for the PAR, Design rule and electric rule checking, LVS , Wire length / load estimator, stick diagrams by using CMOS for various combination ckt and Different timing parameters for Asics. Test specification , need for testability, Boundary Scan Test , Faults , Fault simulation , Automatic Test pattern Generation , SCAN test , Built in Self test ,Gate level simulation and IC verification. Tools used for front to back end chip design.

References:

1. Wayne Wolf, “Modern VLSI Design “ by Pearson Education Asia
2. Michael Smith ,”Application Specific Integrated Circuits –“ by Pearson Education Asia
3. Geiger , Allen Strader,”VLSI Design Techniques for Analog and Digital circuits “ McGraw HILL
4. Neil Weste ,” Principles of CMOS VLSI Design “by Pearson Education Asia

504184 ELECTIVE I
NANOTECHNOLOGY

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

The fundamental science behind nanotechnology, bio systems, molecular recognition, quantum mechanics & quantum ideas, optics. Smart materials & Sensors, self healing structures, heterogeneous nano structures & composites, encapsulations, natural nanoscale sensors, electromagnetic sensors, biosensors, electronic noses. Nanostructures, Micro/Nanodevices, Nanomaterials Synthesis and Applications, Molecule-Based Devices.- Introduction to Carbon Nanotubes.- Nanowires.- Introduction to Micro/Nanofabrication.- Stamping Techniques. Methods and Applications. Materials Aspects of Micro- and Nanoelectromechanical Systems,- MEMS/NEMS Devices and Applications. Nanodevices .Scanning Probe Microscopy, Noncontact Atomic Force Microscopy and Its Related Topics.- Low Temperature Scanning Probe Microscopy, Dynamic Force Microscopy.-. Nanolithography, Lithoraphy using photons,electron beams,soft lithography.Bio-medical applications.

References:

1. Springer Handbook of Nanotechnology ISBN: 978-3-540-35172-6
2. Nanotechnology: A Gentle Introduction to the Next Big Idea, Mark ratner,Daniel Rattner, ISBN-10:0-13-101400-5
3. Nanotechnology :Principals &practices, Sulbha K.Kulkarni,Capital publishing company, ISBN:-81-85589-29-1

504184 ELECTIVE I
MACHINE INTELLIGENCE

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Introduction, Soft Computing intelligence, comparison with conventional Artifical Intelligence, soft computing characteristics, Fuzzy sets, Fuzzy rules and Fuzzy inference systems, Different fuzzy Models : Mamdani, Sugeno, Tsu Kamoto, Fuzzy modeling, Least squares methods for system identification, Derivative based optimization.

Neural networks, Adaptive networks, Supervised learning Neural networks, Perceptron, Backpropagation Multilayer perceptron , Radial basis function networks, Learning from reinforcement, Dynamic programming, Competitive learning, Kohonen's self organizing networks, Principle component networks, LVQ, Hopfield networks.

Adaptive Neuro-Fuzzy interface systems, Advanced Neuro-Fuzzy modeling,

Data clustering algorithms, Neuro-Fuzzy control, Fuzzy filtered neural network, Genetic algorithms in game playing.

References:

1. S. R. Jang, C.T. Sun, E. Mizutani,' Neuro-Fuzzy and Soft Computing', Pearson Education, ISBN 81-297-0324-6.
2. B. Kosko, 'Neural Networks and Fuzzy Systems : a dynamical systems approach' Prentice Hall Publication.
3. Simon Haykin, ' Neural Networks : comprehensive foundation', Prentice Hall, ISBN-10: 0132733501.
4. Jacek M. Zurada , 'Introduction to Artifical Neural Systems', Jaico publications

504185 ELECTIVE II
RECONFIGURABLE COMPUTING

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Computing requirements, Area, Technology scaling, Instructions, Custom Computing Machine, Overview, Comparison of Computing Machines. Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUT's, LUT Mapping, ALU and CLB's, Retiming, Fine-grained & Coarse-grained structures; Multicontext; Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories, Arrays for fast computations, CPLDs, FPGAs, Multicontext, Partial Reconfigurable Devices; TSFPGA, DPGA, Mattrix; Best suitable approach for RD; Case study. Control Logic, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Best suitable methods for RD; Contexts, Context switching; Area calculations for PE; Efficiency, ISP, Hot Reconfiguration; Case study. Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research; Software challenges in System on chip; Testability challenges; Case studies. Modelling , Temporal portioning algorithms, Online temporal placement, Device space management, Direct communication, Third party communication, Bus based communication, Ckt switching, Network on chip, Dynamic network on chip, Partial reconfigurable design.

References:

1. Andre Dehon, "Reconfigurable Architectures for General Purpose Computing".
2. IEEE Journal papers on Reconfigurable Architectures.
3. "High Performance Computing Architectures" (HPCA) Society papers.
4. Christophe Bobda, "Introduction to Reconfigurable Computing", Springer Publication.
5. Maya Gokhale, Paul Ghaham, "Reconfigurable Computing", Springer Publication.

504185 ELECTIVE II
MEMORY TECHNOLOGIES

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs; DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM, High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing. General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.

References:

1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Memories", Springer Publication.
3. Wen C. Lin, "Handbook of Digital System Design", CRC Press.

504185 ELECTIVE II
VLSI EDA TOOLS

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

ASIC design flow, various design entries, IP cores, cross compilers, cell design, stick diagrams, synthesis, place and route, floor planning, power estimation, static timing analysis, dynamic timing analysis, antenna rules, design rule check, electric rule check, schematic rule check, Clock domain crossing check, layout verses schematic, layout techniques, verification, manufacturing tests. Xilinx ISE, Actel libero, Active HDL, Sinplify pro, Leonardo spectrum, Quartus, Boole Dozer, Model Sim- design entries, various simulation, synthesis, place and route, timing verification. Cadence, IC station – design entries, simulations, various tools in the suit, GDS files. Microwind, Spice, Magic – layout techniques, simulations, DRCs, , tools available in the suit.

References:

1. Michael Smith, “Application Specefic Integrated Circuits”, Person Education Asia.
2. Reference manuals of the respective tools.

504186 VLSI EMBEDDED PRACTICE I

Teaching Scheme	Examination Scheme
Practical: 6 Hrs./Week	TW: 50 Marks
	Credit: 3

The faculty associate with instruction of these subjects shall assign laboratory practices to the students, minimum three per course.

The laboratory practices shall encompass implementation/ deployment of the course work in terms of the hardware setup, algorithm development and programming assignment. The student shall submit a document as a bonafide record of such assignment in the hard/soft copy format to the concerned faculty for further evaluation.

504188 REAL TIME OPERATING SYSTEMS

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++, Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance, Operating System Concepts, Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts. Operating system structure Monolithic Systems: Layered Systems, Virtual Machines, Exo-kernels, Client-Server Model,Real Time Operating Systems (µC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting µCos-II. Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management.

References:

1. µC/OS-II, The real time Kernel, Jean J. Labrossy, Lawrence: R & D Publications.
2. Embedded Real Time Systems: Concepts, Design & Programming, Dr.K.V.K.K. Prasad, Dreamtech Publication.
3. An Embedded Software Primer, David E. Simon, Pearson Education Publication.
4. Modern Operating Systems, Second Edition, Andrew S. Tanenbaum, Prentice Hall Publication.
5. Embedded Systems Architecture, Programming and design, Raj Kamal, Tata MCgraw-Hill Publication.

504189 EMBEDDED SIGNAL PROCESSING

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Digital Signal Processing Overview, Convolution, Correlation, Digital filters, DFT, STFT, DCT, wavelets and filter banks, FFT algorithms and Implementation, Representations of the DSP algorithms, Block diagrams, Signal flow graph, Data-flow graph, Dependence graph, iteration bounds, Pipelining and Parallel processing of FIR filters, Algorithm transformation: Retiming , Folding, Unfolding, Algorithmic strength reduction in Filters and Transforms, Parallel FIR filters, Fast FIR algorithms, Discrete cosine transform and Inverse DCT, Parallel processing for IIR filters, Pipelined adaptive digital filters. Introduction to Digital signal processing systems, MAC, Barrel shifter, ALU, Multipliers, Dividers, DSP processor architecture, Software developments, Selections of DSP processors, real time implementation considerations, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, On chip resources, programming considerations, Real time implementations, Applications of DSP systems: FIR filters, IIR filters, DTMF generation and detection, FFT algorithms, wavelet algorithms, Adaptive algorithms: system identification, inverse modeling, noise cancellation, prediction.

References:

1. Sen M. Kuo and Woon-Seng Gan, " Digital Signal Procesors, architectures, implementations, and applications", Prentice-Hall, ISBN 0130352144.
2. V. Madisetti, " The Digital Signal Processing Handbook", IEEE press, ISBN 0849385725
3. K. K. Parhi, "VLSI Digital Signal Processing Systems- Design and Implementation", John Wiley & Sons, Inc.
4. Sanjit K. Mitra, " Digital Signal Processing: A Computer based approach", McCraw Hill, 1998, ISBN 070429537
5. Lawrence R. Rabiner and Bernard Gold, "Theory and application of Digital signal Processing", Prentice-Hall of India, 2006..

504190 RF IC DESIGN

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

I ntroduction to MOSFET Devices, MOSFET modeling, Spice model, Device parasitics, RF modeling, Parasitics sensitive to RF. Issue in RF IC a brief review, Impedance matching, use and design of passive circuits, LNA Design, Matching Techniques using algebra techniques, Basic Bond circuits, UHF Mixer design.Cross talk, Cross connect architecture, Cross Connect characteristics, classification, Cross connect mechanism, Cross connect mitigation, Cross connect reduction, multiple Cross connect sources. EMI, EMC, Importance in ASIC Design, Introduction, EDA Tool in ASIC Design, Design Flow, testing, Environment, sources of EMI/ RFI, Solutions.

References

1. Thomas Lee, " RF IC Design" Oxford Press..
2. T. Yettrdal, Yunhg Cheng, "Devices modeling for analog and RF COMS circuits designe", John Wiley publication 2003.
3. Calvin Plett, "Radio frequency Integrated Circuits Design", Artech house.

504191 ELECTIVE III

FAULT TOLERANT SYSTEM DESIGN

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Modeling: Basic Concept, Functional modeling at the logic level, Functional models at the register level, Structural models, Level of modeling. Type of simulation, unknown logic value, compiled simulation, Event-driven simulation and Hazard Detection. Logical fault models, Fault detection and redundancy, Fault equivalence and fault location, Fault Dominance, Single stuck-fault models, multiple stuck fault model, stuck RTL variables, Fault variables. Testing for Single Stuck fault and Bridging fault. General fault simulation techniques, Serial Fault simulation, Parallel fault simulation, Deductive fault simulation, Concurrent fault simulation, Fault simulation for combinational circuits, Fault sampling, Statistical fault analysis. General aspects of compression techniques, ones- count compression, transition – count compression, Parity – check compression, Syndrome testing and Signature Analysis Basic concepts , Multiple – Bit Errors , Checking circuits and self checking , self – checking checkers , Parity – check function , totally self-checking m/n code checkers , totally self-checking equality checkers , Self-checking Berger code checkers and self checking combinational circuits.Built In Self Test, Self testing circuits for systems, memory & processor testing, PLA testing, Automatic test pattern generation and Boundary Scan Testing JTAG

References:

1. M.Abramovici, M.A. Breuer, A.D. Friedman, “Digital systems testing and testable design”, Jaico Publishing House.
2. Diraj K. Pradhan, “Fault Tolerant Computer System Design”, Prentice Hall.

504191 ELECTIVE III

BIOMEDICAL SIGNALS AND SYSTEMS

Teaching Scheme **Examination Scheme**
Lectures: 3 Hrs./Week **Theory: 100 Marks**
Credit: 3504191

Introduction to Biomedical Signals,Nature of Biomedical Signals, Examples of Biomedical Signals – EMG, ECG, EEG, ERPs,PCG,VMG, VAG, Objectives of Biomedical Signal Analysis, Difficulties in Biomedical Signal Analysis, Concurrent, Coupled, and Correlated Processes- Illustration of the Problem with Case-Studies. Filtering for Removal of Artifacts- Illustration of the Problem with Case-Studies,Time-Domain Filters, Frequency-Domain Filters, Optimal Filtering, The Wiener Filter, Adaptive Filters for Removal of Interference, Selecting an Appropriate Filter Application: Removal of Artifacts in the ECG, Event Detection, Detection of Events and Waves, Correlation Analysis of EEG channels, Cross-spectral Techniques. The Matched Filter, Detection of the P Wave, Homomorphic Filtering, Application- ECG Rhythm Analysis, Identification of Heart Sounds, Waveshape and waveform Complexity, Analysis of Event-related Potentials, Morphological Analysis of ECG Waves, Envelope Extraction and Analysis of Activity, Application- Normal and Ectopic ECG Beats, Analysis of Exercise ECG. Frequency-domain Characterization The Fourier Spectrum, Estimation of the Power Spectral Density Function, Measures Derived form PSDs. Modeling Biomedical Systems, Point Processes Parametric System Modeling Autoregressive of All-pole Modeling, Pole-Zero Modeling, Electromechanical Models of Signal Generation, Application-Heart-rate Variability, Spectral Modeling and Analysis of PCG. Analysis of Nonstationary Signals, Time-Variant Systems, Fixed Segmentation, Adaptive Segmentation, Use of Adaptive Filters for Segmentation, Application- Adaptive Segmentation of EEG Signals, Adaptive Segmentation of PCG Signals. Pattern Classification and Diagnostic Decision , Pattern Classification, Supervised Pattern Classification, Unsupervised Pattern Classification, Probabilistic Models and Statistical Decision , Logistic regression Analysis The Training and Test Steps, Neural Networks, Measures of Diagnostic Accuracy and Cost, Reliability of Classifier and Decisions

References:

1. R. M. Rangayyan “Biomedical Signal Analysis- A case study approach”, Wiley Publications.
2. Eugene N Bruce “Biomedical signal processing and signal modeling”, Wiley publications.

504191 ELECTIVE III

ADVANCED DIGITAL SYSTEM DESIGN

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Digital System Design aspects for RISC and CISC CPU architectures. Control and Data path units of Processor. Practical design aspects for high frequency digital design such as clock skew and synchronous / asynchronous input signal handling. Hazard analysis, fault tree analysis. Estimation of digital system reliability. System integrity. Design of digital system for network applications such as ATM switch design, ATM packet generator, ATM packet decoder. Hardware testing and design for testability: Testing combinational and sequential logic, scan testing, boundary scan and BIST. VHDL models for memories and buses such as SRAM memory, 486 bus model and memory interfacing with microprocessor bus. Floating point arithmetic operations such as multiplications and others. Digital system design for asynchronous serial data transfer.

References:

1. John F. Wakerly,"Digital Design principles and practices",3rd edition, PHI publications.
2. Charles H. Roth, "Digital system design using VHDL", Thomson Publication.
3. Balabanian,"Digital logic design principles",Wiley publication.
4. Stephen Brown, "Fundamentals of digital logic", TMH publication.

504192 ELECTIVE IV (OPEN)
EMBEDDED AUTOMOTIVE SYSTEMS

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Current trends in Automobiles, open loop and closed loop systems - components for electronic engine management system. Electro magnetic interference suppression. Electromagnetic compatibility, Electronic dashboard instruments, onboard diagnostic system , security and warming system. Electronic management of chassis systems. Vehicle motion control. Sensors and actuators, and their interfacing. Basic sensor arrangement, types of sensors such as- oxygen sensors, crank angle position sensors- Fuel metering/ vehicle speed sensors and destination sensors, Attitude sensor, Flow sensor, exhaust temperature, air mass flow sensors. Throttle position sensor, solenoids, stepper motors, relays. Electronic ignition systems. Types of solid state ignition systems and their principle of operation. Digital engine control system. Open loop and closed loop control system, Engine cranking and warm up control. Acceleration enrichment. Deceleration learning and ideal speed control, Distributor less ignition – Integrated engine control system, Exhaust emission control engineering. Automotive Embedded systems. PIC, Freescale microcontroller based system. Recent advances like GLS, GPSS, GMS. Multiprocessor communication using CAN bus. Case study- cruise control of car. Artificial Intelligence and engine management.

References:

1. William B. Riddens, “Understanding Automotive Electronics”, 5th Edition, Butterworth Hennimann Woburn, 1998.
2. Young A.P. & Griffiths, “ Automotive Electrical Equipment” , ELBS & New Press-1999.
3. Tom Weather Jr. & Cland c. Ilunter, “ Automotive computers and control system” Prentice Hall Inc., New Jersey.
4. Crouse W.H., “ Automobile Electrical Equipment” , Mc Graw Hill Co. Inc., New York ,1995.
5. Bechhold, “ Understanding Automotive Electronic”, SAE,1998.
6. Robert Bosch,” Automotive Hand Book”, SAE (5TH Edition),2000.

504192 ELECTIVE IV (OPEN)
SYSTEM-ON-CHIP (SoC)

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

IC Technology, Economics, CMOS Technology overview, Power consumption, Hierarchical design, Design Abstraction, EDA tools. MOSFET model, parasitics, latch up, advanced transistor structures; Wire parasitics; Design rules, Scalable design rules, process parameters; stick diagrams, Layout design tools; Layout synthesis, layout analysis. CMOS gate delays, transmission time, speed power product, low power gates; Delay by RC trees, cross talk, RLC delay, cell based layout, Logic & interconnect design, delay modeling, wire sizing; Power optimization, Switch logic networks. Pipelining, Data paths, Adders, ALUs, Multipliers, High density memories; Metastability, Multiphase clocking; Power optimization, Design validation, Sequential testing; Architecture for low power. Floor planning methods, global routing, switch box routing, clock distribution; off chip connections, packages, I/O architectures, pad design. Complete chip design including architecture, logic and layout for Kitchen timer chip OR Microwave oven chip.

References

1. Wayne Wolf, “Modern VLSI Design”, Pearson Education.
2. Kamaran Eshraghian, “Principles of CMOS VLSI Design”, Pearson Education
3. Rabey, Chandrakasan, “Digital IC Design”, Preason Publication.

504192 ELECTIVE IV (OPEN)
SOFTWARE DEFINED RADIO

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

SDR concepts & history, Benefits of SDR, SDR Forum, Ideal SDR architecture, SDR Based End-to-End Communication, Worldwide frequency band plans, Aim and requirements of the SCA, Architecture Overview, Functional View, Networking Overview, Core Framework, Real Time Operating Systems, Common Object Request Broker Architecture (CORBA), SCA and JTRS compliance, Radio Frequency design, Baseband Signal Processing, Radios with intelligence, Smart antennas, Adaptive techniques, Phased array antennas, Applying SDR principles to antenna systems, Smart antenna architectures, Low Cost SDR Platform, Requirements and system architecture, Convergence between military and commercial systems, The Future For Software Defined Radio

References:

1. Dillinger, Madani, Alonistioti (Eds.): Software Defined Radio, Architectures, Systems and Functions, Wiley 2003
2. Reed: Software Radio, Pearson
3. Software Defined Radio for 3G, 2002, by Paul Burns.
4. 4.Tafazolli (Ed.): Technologies for the Wireless Future, Wiley 2005
5. Bard, Kovarik: Software Defined Radio, The Software Communications Architecture, Wiley 2007

504193 VLSI EMBEDDED PRACTICE II

Teaching Scheme	Examination Scheme
Practical: 6 Hrs./Week	**TW: 50 Marks**
	Credit: 3

The faculty associate with instruction of these subjects shall assign laboratory practices to the students, minimum three per course.

The laboratory practices shall encompass implementation/ deployment of the course work in terms of the hardware setup, algorithm development and programming assignment. The student shall submit a document as a bonafide record of such assignment in the hard/soft copy format to the concerned faculty for further evaluation.